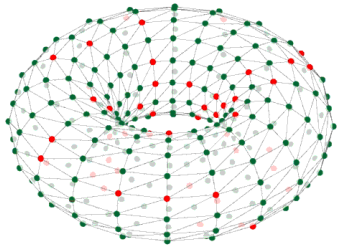
SpiNNaker Hardware & Software



Overview

SpiNNaker Workshop
September 2016

European Research Council
Established by the European Commission

Human Brain Project

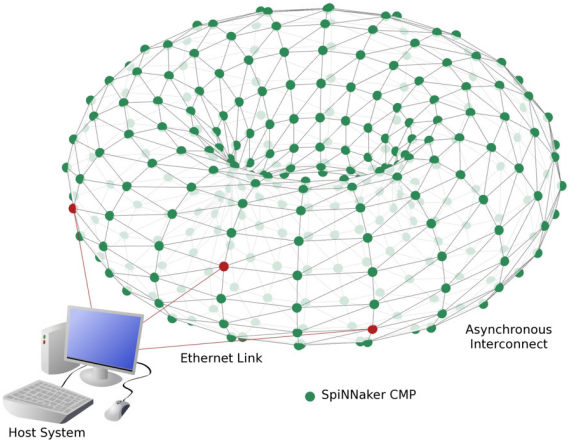
EPSRC

SpiNNaker

Contents

- What is SpiNNaker?
- SpiNNaker at different scales
- SpiNNaker architecture: chip & system
- Using SpiNNaker

SpiNNaker Project

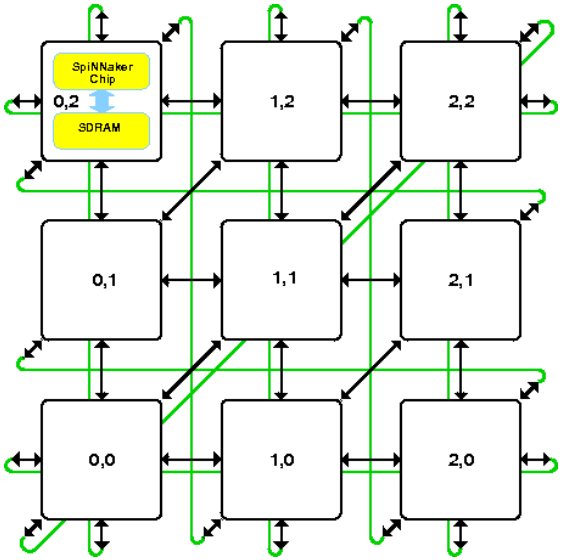


A million mobile phone processors in one computer
Able to model about 1% of the human brain…
…or 10 mice!

How is SpiNNaker Used?

- Some key user communities:
  - **Computational neuroscientists** to simulate large neural models and try to understand the brain
  - **Roboticists** to build advanced neural sensory and control systems
  - **Computer architects** to apply neural theories of computation to non-neural problems

SpiNNaker System



Chip-to-chip communications: Packet routing

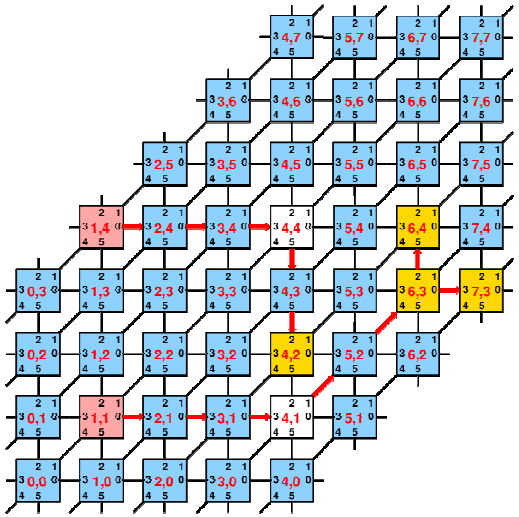
- No memory shared between chips!
- Communicate via simple messages called ***packets:***
  - *40 bit (no data) or*
  - *72 bit (includes 32-bit data word)*
- Four types of routing, most important (for you) is ***multicast***
- Packets used to communicate with the host and external peripherals:
  - Via Ethernet adapter for host comms.
  - Or via chip-to-chip SpiNNaker links for external devices

Routing Types

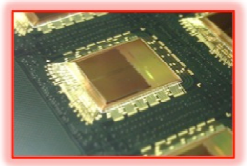
Nearest Neighbour
Point-to-Point
Multicast
Fixed Route

Multicast Routing

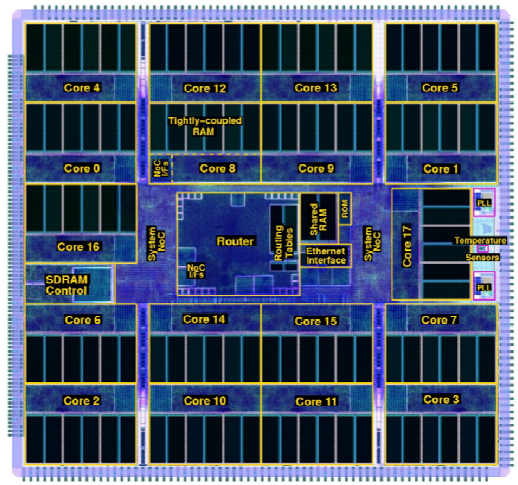
- Hardware router on each node
- Packets have a routing key
- Router has a look-up table of {*key, mask, data*} triplets
- If address matches a *key-mask* pair, the associated *data* tells router what to do with the packet



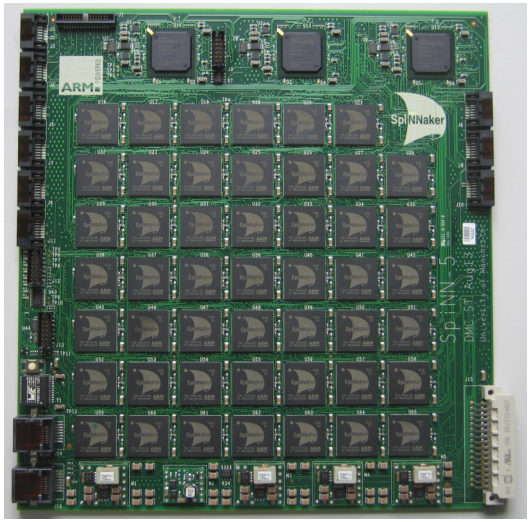
SpiNNaker Chip

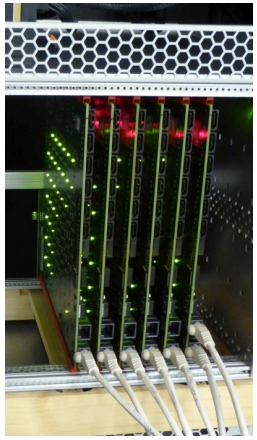


Multi-chip packaging by UNISEM Europe



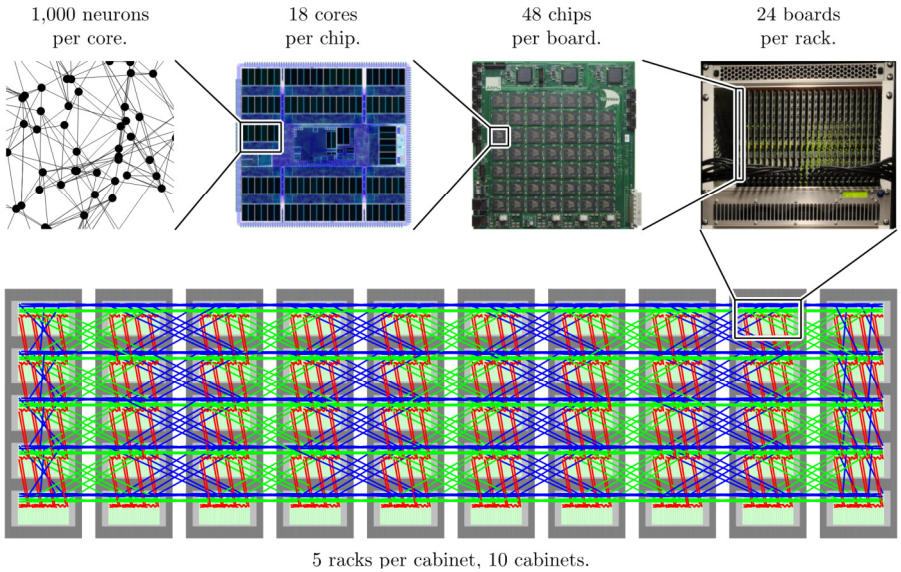
SpiNNaker Boards





SpiNNaker Machines

Scaling to a billion neurons



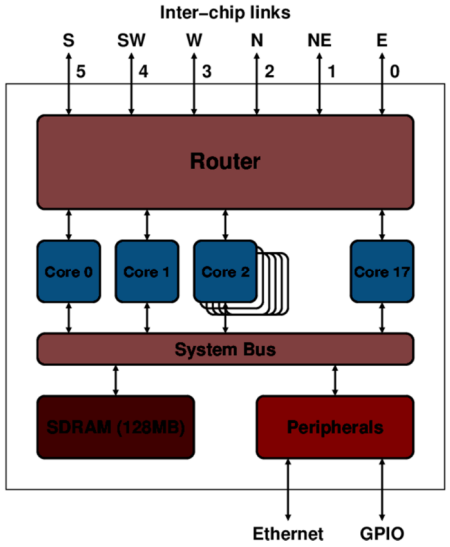
What Next for SpiNNaker?

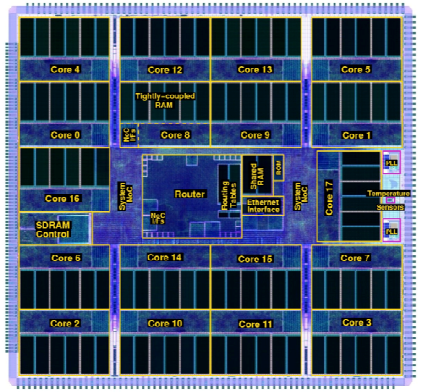
- Five cabinet machine (500K ARM cores)
  - Now online and available!
  - Open to any research project, in principle
- SpiNNaker2 being developed within HBP
  - New systems by 2020?
- For further information contact:

simon.davidson@manchester.ac.uk

Chip Architecture

SpiNNaker Node





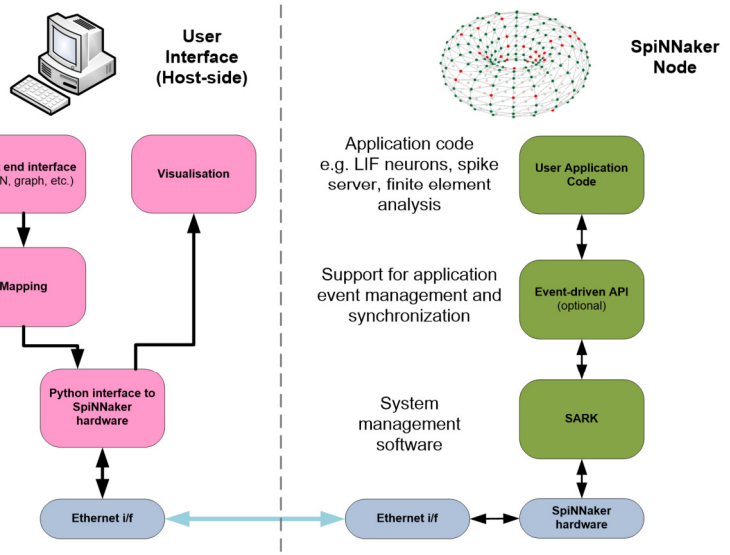
Chip Resources

- 18 cores on a chip:
  - 1 Monitor Processor
  - 16 Application processors
  - 1 fault-tolerant/yield spare
- Each core is an ARM968 processor
  - 200 MHz clock speed
  - No memory management or floating point!
  - Local memories:
    - 32K local code memory (ITCM), 64K local data (DTCM)
    - TCMs are visible only to local processor
- 128MByte SDRAM
  - Shared and visible to all processors on **same node**
- Router:
  - Directs flow of information from core-to-core across the machine

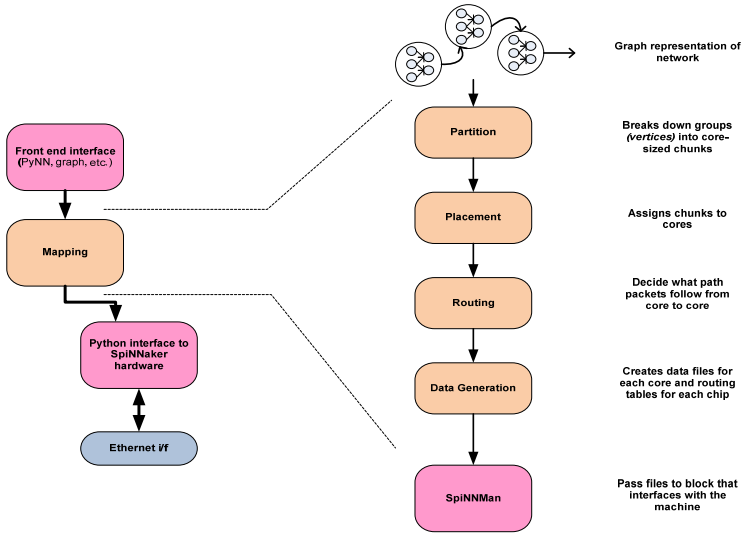
Using SpiNNaker:

The Software Stack

Software Stack



Mapping Process



What Files are Required for Simulation?

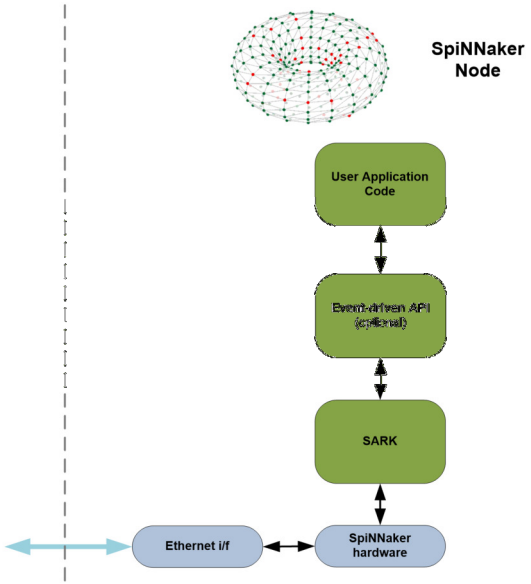
Files Required

For Each Core (16 per chip):

- Application C executable (32KB)
- Application local data (64KB)
- Application shared data (8MB)

For Each Chip:

- Router table
- Any shared data tables



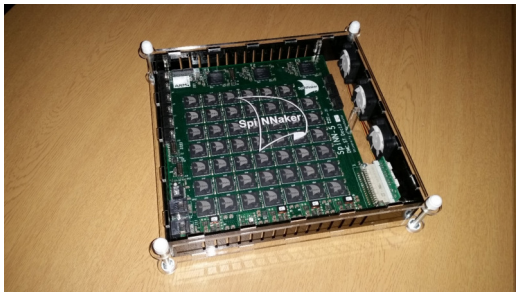
Order of Events (batch mode)

1. Compile network description
2. Map graph to machine
3. Generate data files
4. Load files
5. Synchronise the start on all cores!
6. Simulation runs to completion
7. Hands back control to host
8. Read back results and post-process

End of Overview!

- Much more detail on all of these topics
  - In the sessions to come….
- Any questions for now?
- Just one more thing to add….

Buying SpiNNaker Hardware



- 48-node board now available for sale
- Non-commercial use only
- 4-node boards can only be loaned (currently!)

- For further information contact: simon.davidson@manchester.ac.uk