AppNote 1 - SpiNN-3 Development Board

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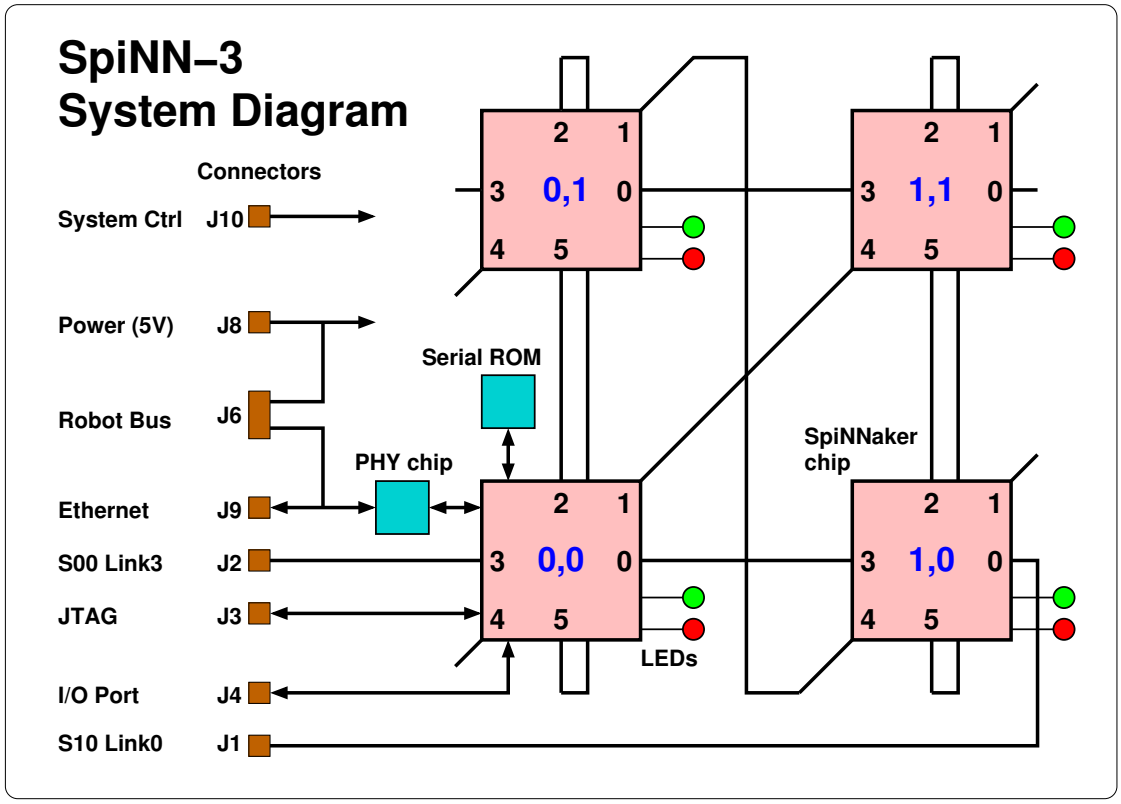
Steve Temple - 24 Nov 2011 - Version 1.00

Introduction

This document is a brief introduction to the SpiNN-3 Development Board hardware. The board houses 4 SpiNNaker chips each of which contains 18 ARM968 processing cores with local memory. The chips also contain a 1 Gbit (128 Mbyte) SDRAM device. Each chip has 6 bidirectional communication links and the four chips are connected together using these links. One chip, labeled "0,0" is notionally the master chip and it has a number of external interfaces.



The master chip is equipped with a serial ROM chip which contains some networking parameters (MAC address, etc) and which can be used to bootstrap the system with specialised software. Normally, the chips boot from an internal ROM. The master chip has an Ethernet interface provided via an external PHY chip which can run at 10 or 100 Mbit/s. There is a standard RJ45 socket to connect to a network.

The chips have JTAG connections and a JTAG port is available on a connector. Each chip has two LEDs, one red and one green, which can be driven from an I/O port. The master chip has a further 8 bits of its I/O port brought out to a connector. The board may be reset via a push-button switch and there is further connector to allow the board to be remotely reset.

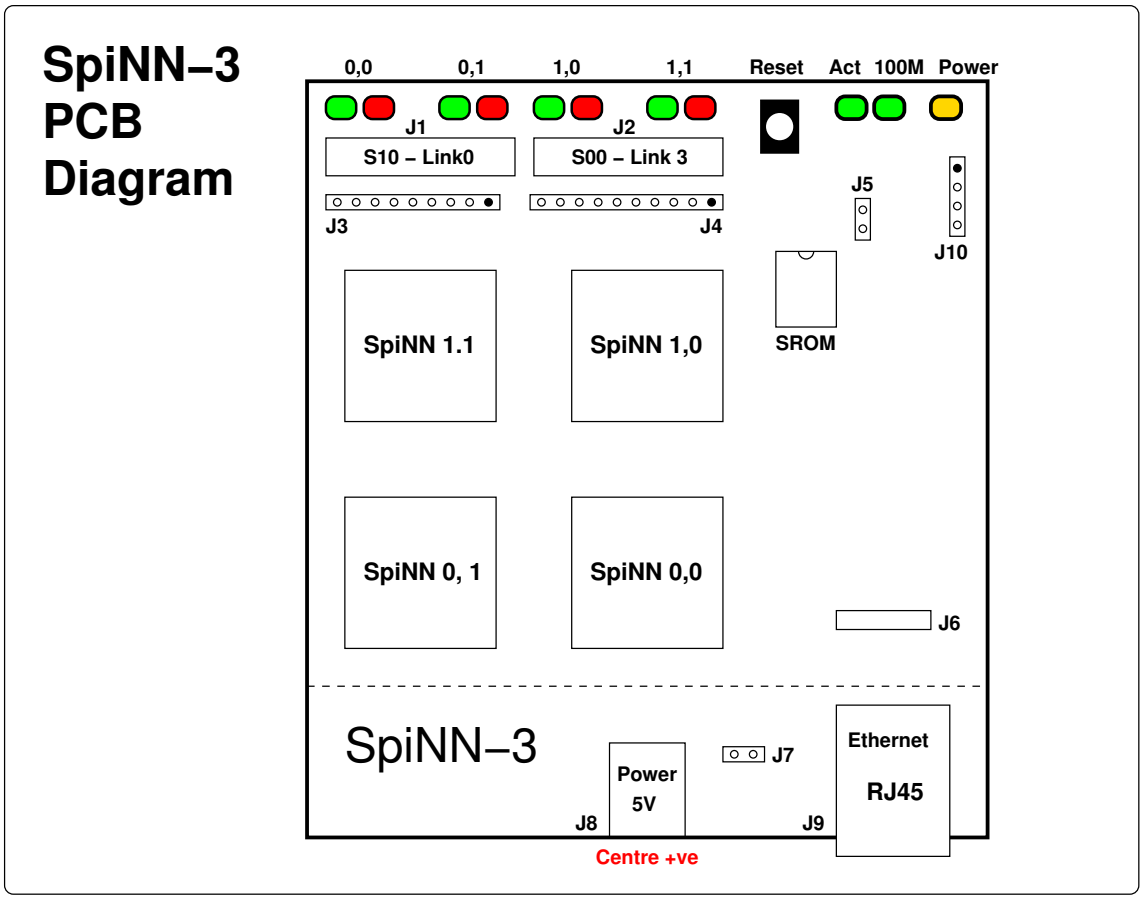
Two of the communication links are available on connectors to allow boards to be connected together or for attaching peripherals. Link 3 on chip "0,0" is available as well as link 0 on chip "1,0".

One of the anticipated uses for the board is in an autonomous robot. In this application, a

section of the PCB is cut off and the board connects to the robot via a specialised connector which provides power and Ethernet connections.

Physical Details

The board is a 1.6mm thick, 6-layer FR4 PCB measuring 90 by 100mm. When used in a robot, 20mm is removed (losing connectors J8 and J9) and the board is then 90 by 80mm. The board may be supplied with its assembly tooling bars still attached as this gives room to attach rubber feet. The tooling bars may be removed if they are not needed.



Power Supply

The board requires a single 5V, 1A supply which is provided via a standard 2.1mm DC power socket (J8). The centre pin is the positive rail. When idle, the card draws about 400mA but peaks at around 1A for a few milliseconds when the board powers up and goes through its self-test routines. Please ensure that the correct supply is used as the card has no protection from over-voltage or reversed polarity.

Internally, the board has devices running at 3.3V, 1.8V and 1.2V. The 3.3V supply is derived using a linear regulator on the 5V rail and the 1.8V supply is derived by a linear regulator on the 3.3V rail. The 1.2V supply, which supplies the core circuitry for the SpiNNaker chips, is derived from the 5V rail by a switching DC-DC converter module.

When configured for use in a robot, two supplies of 3.3 and 5V are provided via the robot connector (J6).

Ethernet Connection

The board uses Ethernet to connect with a host machine which is used to download code and to communicate with executing code. The PHY chip which is used can operate at 10 or 100 Mbit/s and switches automatically when connected to an Ethernet hub or switch.

The MAC address for the board and the IP address are contained in the serial ROM. These will normally be pre-programmed but it is possible to change them using the host interface software. Static IP addresses are normally used but there is an experimental DHCP implementation available.

LEDs

Each SpiNNaker chip has two LEDs connected to its I/O port. A green LED is connected to bit 0 and a red LED to bit 5. The port outputs need to be driven low to turn the LEDs on. Note that the red LED I/O bit on the master chip is shared with the serial ROM so it will turn on while the serial ROM is being accessed.

A yellow LED in the top right corner of the board is driven from the 5V supply rail and indicates that the board is powered. There are also two green LEDs beside the power LED which are attached to the PHY chip. The RJ45 connector also contains 2 LEDs connected in parallel with these. One is turned on when a 100 Mbit/s link is present. The other is turned on when an active link is detected and flashes when packets are received.

Connectors and Interfaces

There are 10 connectors and links on the board. Where pin 1 is not obvious from the PCB silk screen or the connector itself, refer to the PCB diagram where pin 1 is marked by a solid black circle. There are five connectors which provide direct access to the SpiNNaker chips. These are J1 and J2 which provide access to two communication links, J3 which is the JTAG port, J4 which is an I/O port and J10 which is a reset port which allows an external device to reset the board. All of these connectors operate using LVCMOS levels at 1.8V though the inputs are 3.3V tolerant.

Conn.	Function
J1	Chip "1,0" - link 0
J2	Chip "0,0" - link 3
J3	JTAG port
J4	I/O port
J5	Select alternative Boot ROM
J6	Robot interface
J7	(Testing use only)
J8	5V power input
J9	Ethernet RJ45
J10	Reset port

JTAG Port

The JTAG port contains the standard JTAG signals (TMS, TCK, TDI and TDO) as well as a returned clock signal (RTCK) and a JTAG reset input (NTRST). An active-low system reset signal (NSRST) is also available which drives the power-on reset input of all 4 SpiNNaker chips. Finally, the 1.8V supply rail is also present to act as voltage reference for the JTAG driver.

The JTAG ports on the four chips are daisy-chained chained in the order "0,0" to "0,1" to "1,0" to "1,1". Chip "0,0" is at the head of the chain.

Pin	**JTAG Port Function**
1	1.8V
2	NTRST
3	TDI
4	TMS
5	TCK
6	RTCK
7	TDO
8	SNRST
9	GND

I/O Port

The I/O port brings out 8 GPIO lines from the master SpiNNaker chip. When the system is reset the lines are all configured as inputs and have pull-down resistors active. Each line may be configured as an output and have its pull-down resistor disconnected by software. Two of the lines also act as interrupt lines inside the chip which are routed to all CPUs via interrupt controllers.

When configured as outputs, up to 4mA may be sourced or sunk. As inputs, the lines have LVCMOS thresholds and are 3.3V tolerant. The nominal operating voltage of the I/O port is 1.8V.

Pin	**I/O Port Function**
1	1.8V
2	GPIO[15]
3	GPIO[14]
4	GPIO[13]
5	GPIO[12]
6	GPIO[11]
7	GPIO[10]
8	GPIO[9] / INT[3]
9	GPIO[8] / INT[2]
10	GND

Reset Port

The Reset port brings out a small number of control lines to allow the board to be remotely reset. The same system-wide reset input as appears on the JTAG connector is provided as are the user reset input (RST) and 32kHz clock input (CLK32). These signals are connected to all 4 SpiNNaker chips.

Pin	**Reset Port Function**
1	RST
2	CLK32
3	SNRST
4	GND

Power-Up and Troubleshooting Guide

On connecting a 5V supply to the board, the yellow power LED should come on immediately. The Spinnaker chips have a power-on reset circuit which should reset the SpiNNaker chips at this

point and they will begin executing their bootstrap code from internal ROM. If this is successful, they start flashing their green LEDs at 1Hz. If the power supply ramps up too slowly, the power-on reset circuit may not function correctly but pressing the reset button should always reset the chips and result in four flashing green LEDs. If the board does not appear to reset correctly, ensure that the power supply can provide the 1A that the board needs to start up.

If a serial ROM is present (as is usually the case), the red LED attached to the master chip will turn on while the ROM is being read after reset. Depending on the contents of the ROM this may just be a brief flash (a few ms) or may be longer (a second or two).

When an Ethernet cable is attached to the board the green LED next to the reset switch (the Activity LED) should come on. If a 100 Mbit/s link is being used, the other green LED next to the power LED should also come on. The Activity LED will flash when an Ethernet packet is received by the board.

Once connected to the Ethernet, the board should respond to ICMP pings sent to its IP address and the Activity LED should flash as packets arrive. If the board behaves as described above, it is probably functional and ready to connect to a host system.

Change log:

- *1.00 - 24nov11- ST* - initial release - comments to *temples@cs.man.ac.uk*