AppNote 9 - SpiNN-5 Quick Start Guide

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Steve Temple - 12 Feb 2015 - Version 1.02

Introduction

This note is a quick-start guide to the SpiNN-5 circuit board. It's meant to allow you to get the board up and running without going into too much detail about how everything works.

The board houses 48 SpiNNaker chips which are connected in a hexagonal arrangement and interconnected via 6 bidirectional SpiNNaker communication links per chip. The board also has 3 Spartan6 FPGAs which can provide board-to-board interconnection of external SpiNNaker links using SATA hardware. A diagram of the board appears below.
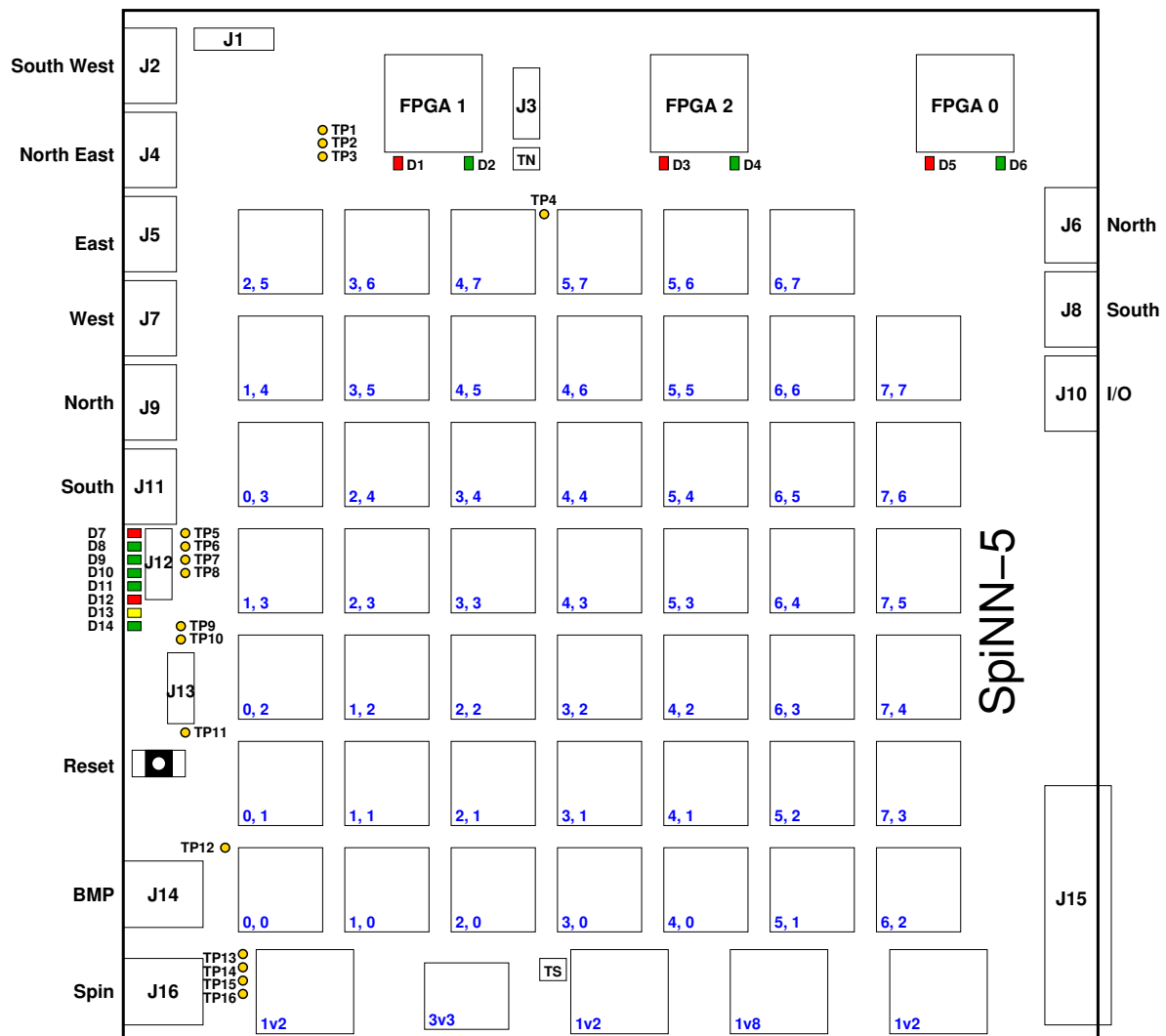
Single boards are generally supplied in one of two forms - boxed or open. In the latter case a backplane will also be provided. If you have been provided with a single SpiNN-5 board then you should also have been given a power supply.

The board requires a 12V DC supply at up to 6A and this connects either to a connector at the rear of the box or to any of the three power connectors on the rear of the backplane. If you have

a backplane, the SpiNN-5 board should be plugged into Slot 0 on the backplane which is the right hand socket when viewed from the front. In this case you should ensure that everything is connected **before** you switch power on or off.

The board can get quite warm in operation so it is recommended that open boards are mounted upright so that hot air can easily leave both sides of the board. There are two thermal sensors (TN, TS) on the board which will shut the board down if it becomes excessively hot.

The board is controlled by a Board Management Processor (BMP) which manages much of the board's infrastructure such as power management, clocking and resetting of the SpiNNaker chips and FPGAs.

There are two network interfaces present on connectors J14 and J16. These are standard 100Mbit Ethernet interfaces. J14 is connected to the BMP and J16 is connected to SpiNNaker chip (0,0) at the bottom left of the array of SpiNNaker chips.

A number of LEDs are present on the board which are useful for observing the state of the system. Each FPGA has two LEDs (D1-D6) while the BMP has 8 LEDs (D7-D14). Each SpiNNaker chip has a single LED mounted on the back of the board.

A reset switch is present which resets the BMP and provides a complete restart of the board. In the boxed system, the reset switch can be activated through a slot in the case using a non-conducting implement or the board can be power cycled to achieve the same effect.

Power-Up and Troubleshooting Guide

After applying power the board should reset and commence operation. If this doesn't seem to happen it may be that the power supply has ramped up too slowly and you can use the reset switch to force a board reset.

If the BMP is operating normally, then the bottom green LED (D14) should flash once per second. Following reset, the BMP will configure the FPGAs and this should cause one or both of the LEDS on each FPGA to come on and/or flash.

The yellow LED, D13, indicates that the BMP has applied power to the SpiNNaker chips and the FPGAs and should normally be turned on. (This LED is orange/red on some early boards). If the SpiNNaker chips have been correctly powered and reset then they will flash their LEDs once every two seconds. These LEDs are not initially synchronised and will appear to flash with random phase.

The red LED, D12, is used to warn of some potential problems with power supplies and/or cooling. It may flash on a single board but this is not necessarily a cause for concern.

A software problem on the BMP will cause red LED D7 to come on and in this case an error code may be placed on green LEDs D8 to D11. This is normally an indication that the board needs attention.

If the board appears to be operating correctly, then you can attach network cables to both network interfaces and check that they are functional (see below for information on IP addresses). Both interfaces should respond to `ping` packets. The reception of a packet on the BMP interface will also cause LED D8 to flash briefly.

If both interfaces are responding to `ping` the board is probably functional and ready for use. Note that the BMP interface is not required for normal operation of the board but does allow remote resetting of the SpiNNaker chips as well as various system monitoring functions.

IP Addresses

Each of the two network interfaces on a SpiNN-5 board has its own IP address (as well as MAC address, gateway address and net mask). The board has default values for these parameters which may be overridden by explicit configuration. In this case the parameters are stored in non-volatile (flash) memory in the BMP.

In the default case, the values used depend on whether or not the board is housed in a backplane. When in a backplane, the network settings are taken from a memory device on the backplane. When not in a backplane, the following settings are used

```
SpiNNaker IP      192.168.240.1
SpiNNaker GW      192.168.240.254
SpiNNaker NM      255.255.0.0
SpiNNaker MAC     00:00:a4:f0:00:01
BMP IP            192.168.240.0
BMP GW            192.168.240.254
BMP NM            255.255.0.0
BMP MAC           00:00:a4:f0:00:00
```

When you receive your SpiNN-5 board you will also receive notification of the IP addresses which have been configured if they are different from those above. Note that if you use the private IP address ranges above (192.168.x.x) then you should set the net mask on your host computer to 255.255.0.0.

Change log:

- *1.00 - 08apr14- ST* - initial release - comments to *steven.temple@manchester.ac.uk*

- *1.01 - 30may14- ST* - minor text improvements

- *1.02 - 12feb15- ST* - update for boxed version